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Low Power Design Techniques

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Abstract:

The demand for portable electronic devices that offer greater functionality and performance at lower costs and smaller sizes has increased rapidly. This market trend is driving the need for efficient System-on-Chip (SoC) designs, where the power arises as the one of the biggest problems. The microprocessor design has traditionally focused on dynamic power (active power) consumption as the limiting factor in system integration. As technology has shrunk to 90 nm and below, static power (leakage power) is posing new challenges to low power design.

Historically, CMOS technology has dissipated much less power than earlier technologies such as transistor-transistor and emitter-coupled logic. In fact, when not switching, CMOS transistors consumed negligible power. However, with the increase in device speed and chip density, the power of CMOS increased dramatically. According to technology trends, the dynamic power per device decreases over the time. However, if it is assumed that the number of on-chip devices doubles every two years, total dynamic power increases on per-chip basis. Additionally, the shrinking of feature sizes makes static power dissipation grows exponentially. Consequently, the packaging and cooling costs as well as the limited power capacity of batteries become unsustainable.

The reduction of power growth below the predicted numbers has become one of the most important tasks for designers. To cope with the power challenges, a number of advanced power saving techniques have been developed that can efficiently target both static and dynamic power loss. The existing and future trends in low power design show that efficient power management is greatly determined by design decisions made in early phase of system design. Thus, the selection of power saving strategy becomes one of the most important challenges for designers.

This presentation starts by covering basic sources of power consumption in CMOS, including both static and dynamic power loss. Furthermore, the presentation gives a detailed overview on existing low power techniques including standard techniques developed for mature technologies, process-level techniques, and advanced low power techniques used in deep-submicron CMOS. Also, some attention is given to the selection of power saving strategy for design and early power estimation. Finally, future trends in low power design are discussed as well.

Keywords: low power, system-on-chip, dynamic power, static power,

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