First Workshop on Hardware Defined Programming – HDP

Adaptive Computing with Reconfigurable Hardware

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The first workshop on Workshop Hardware Defined Programming (HDP) offers a platform for presenting innovative research topics in the field of reconfigurable computing. Young researches are engaged to present novel approaches and methods addressing the related computer engineering challenges of hardware adaption. The workshop will not only focus on academic research, but also intends to be a forum for tool providers, hardware designers, and application developers.

1 Topics

Our workshop focuses on a wide range of topics in the field of the design of (heterogeneous) hardware architectures, applications and innovations in the area of the necessary design tools. The significant topic cloud computing also provides an outlook on future application areas for reconfigurable hardware. The topics of the workshop are:

- Embedded hardware/software systems and hardware/software codesign
- Supplemental design infrastructures (e.g. Network-on-Chip)
- Design and analysis of energy efficient, heterogeneous architectures
- Hardware accelerators based on reconfigurable hardware such as FPGAs
- Reconfigurable System-on-Chip (RSoC)
- Test, diagnosis, simulation and trace analysis of hardware systems
- High-level synthesis tools, frameworks and specification languages
- Security-critical and cryptographic applications on FPGAs
- Design and analysis of multi-core architectures
- Big data processing with FPGAs and data center integration aspects
- Reconfigurable hardware architectures in cloud environments

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doi:10.18420/in2017_42

2 Contributions

The objective of the workshop is thereby a selection of current research and development in these areas and shall provide a platform for discussing innovative developments and ideas in the field of hardware design. The first HDP workshop includes six contributions, all accepted as full paper with presentation:

I. Applications I – Reconfigurable computing

- FPGA-basierter Protein- und DNA-Sequenzvergleich zur optimierten Datenbanksuche mit dem BLAST-Algorithmus
  Thomas Fabian Starke, Timm Bostelmann and Sergei Sawitzki
- A Hardware Accelerator Framework Approach for Dynamic Partial Reconfigurable Overlays on Xilinx PYNQ
  Benedikt Janßen, Tim Wingender and Michael Hübner

II. Applications II – Hardware/software-codesign

- Modellierung anwendungsspezifischer Hardware und deren Einbettung in die DBT-basierte Prozessor-Verhaltenssimulation
  Steffen Köhler and Rainer G. Spallek
- Hardwaregestützte Positionsschätzung mit Bayes'schen Filtern auf Basis 3-dimensionaler Umgebungsmodelle für den Innenbereich
  Christian Schott, Daniel Froß, Marko Rößler and Ulrich Heinkel
- DC/DC Converter Development by Means of Electrical/Thermal Co-Simulation – from Concept to Control Algorithm and Test
  Radovan Vuletić, Sandra Zeljković, Pawan Garg and Denais Alann

III. Security-critical and cryptographic hardware designs

- A New Level of Trusted Cloud Computing - Virtualized Reconfigurable Resources in a Security-First Architecture
  Paul R. Genßler, Oliver Knodel and Rainer G. Spallek
- Separated Random Number Generators for Virtual Machines
  Clemens Fritzsch, Jörn Hoffmann and Martin Bogdan

3 Summary and Outlook

We thank the organization and the program committee for their collaboration of organizing a successful workshop. We hope to come back next year as well having the 2nd workshop on hardware defined programming (HDP) in 2018.