DC/DC Converter Development by Means of Electrical/Thermal Co-Simulation – from Concept to Control Algorithm and Test

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Abstract: This paper presents the development of 3 kW bidirectional, non-isolated, multiphase interleaved, synchronous 48 V/12 V DC/DC buck-boost converters. It describes solutions for different concept, hardware and software challenges, starting with selection of proper circuit topology, selection of power switches (switching frequency, voltage class and current ratings), calculation of power budget (efficiency) and thermal analysis, Furthermore, it explains PCB layout electrical/thermal co-simulations, elaborating approach in development of average current control algorithm with the target to enable phase shedding and equal current sharing among active phases, improve the light load efficiency and thermal behaviour. Finally, it tackles the topic of automated code generation and implementation on dedicated microcontroller.

Keywords: Multiphase 48 V/12 V DC/DC Converter, Electrical/Thermal Co-Simulation, Average Current Control Algorithm, Automated Code Generation.

1 Introduction and Requirements

Recently, tightening of environmental legislation regarding CO_2 emission has pushed automotive OEMs to intensively think of ways to improve the fuel consumption efficiency by further extending and improving electrification of passenger vehicles. As a result, an additional voltage level, 48 V on-board power network is being introduced [GVRL15]. In this case, although the energy is generated and stored at the 48 V level (48 V battery), the 12 V battery and its loads (lighting, safety functions etc.) have to be supplied using a DC/DC converter, which links these two board nets and enables continuous, safe and efficient bidirectional energy transfer.

An interface converter between 12 V and 48 V board nets has to be capable of bidirectional power transfer from approximately 1.5 kW up to 3 kW. This power rating is primarily a requirement for the power transfer to the 12 V side, and may differ for the

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energy flow in the opposite direction. At 48 V side, the converter faces the voltage range between 36 to 54 V, whereas extended voltage range of 24 V to 60 V should be covered with derating functions. Operating output voltage at 12 V side is specified in the range from 10 V to 16 V. As both 12 V and 48 V are below the safety limitation of 60 V, galvanic isolation is not required and therefore efficiency above 95 % (for load above 250 W) with passive air cooling is targeted. Besides low cost as the primary driver in the automotive industry, requirements of an automotive 48 V to 12 V DC/DC converters include high reliability, high efficiency and modularity. Protection against short circuit between 48 V to 12 V board nets inside the converter itself is essential and needs to be avoided by any means. Additional functions are needed to protect the system against overload, over-temperature and reverse polarity at 12 V side. The most suitable approach, taking high output currents in this application (up to 250 A) into account is a multiphase design [ATA16] of the power stage. Proven advantages of the multiphase design combined with an interleaved switching scheme [GZC09, SL13] are modularity and scalability, improved thermal distribution, reduction of capacitor size as well as the phase shedding to achieve optimal efficiency at partial load. Furthermore, several phases in parallel allow using components with lower current rating.

The important safety-relevant function of disconnecting 48 V from 12 V automotive net in a regular buck topology requires additional protection switches to isolate the failed phase(s) after short-circuit failure of the semiconductor. They have to disconnect the 12 V from 48 V net in case when short circuit occurs at any of MOSFET switches [GB16]. By disconnecting one independent block in case of an internal short circuit in a particular phase, the system can continue delivering the reduced amount of power to the output. Therefore, 50% (one remaining block is operating) of nominal power can still be transferred. Thus, fault-tolerance for short- and open-failures is achieved and operation with reduced number of phases is feasible.

2 Power Converter Design

2.1 Methodology

Power converter is implemented as a multi-stage DC/DC converter made out of 8 interleaved stages, each stage containing same buck/boost topology. Main reason for implementation of relatively high number of power stages, next to the modularity requirement, is lack of commercially available, automotive qualified inductors capable to continuously handle high currents ratings (>30 A_{DC}/10 $A_{p\text{-}p}$).

During the concept phase, the DC/DC converter performance is investigated by means of electrical-thermal co-simulation as depicted on the Fig. 1. MOSFET behavioural SPICE models (models with electrical thermal ports) are used to enable selection of optimal power switches (switching frequency, voltage class/technology and current ratings), calculation of power budget (efficiency) and thermal analysis. Typical example of

parameters variation is shown in Fig. 2.

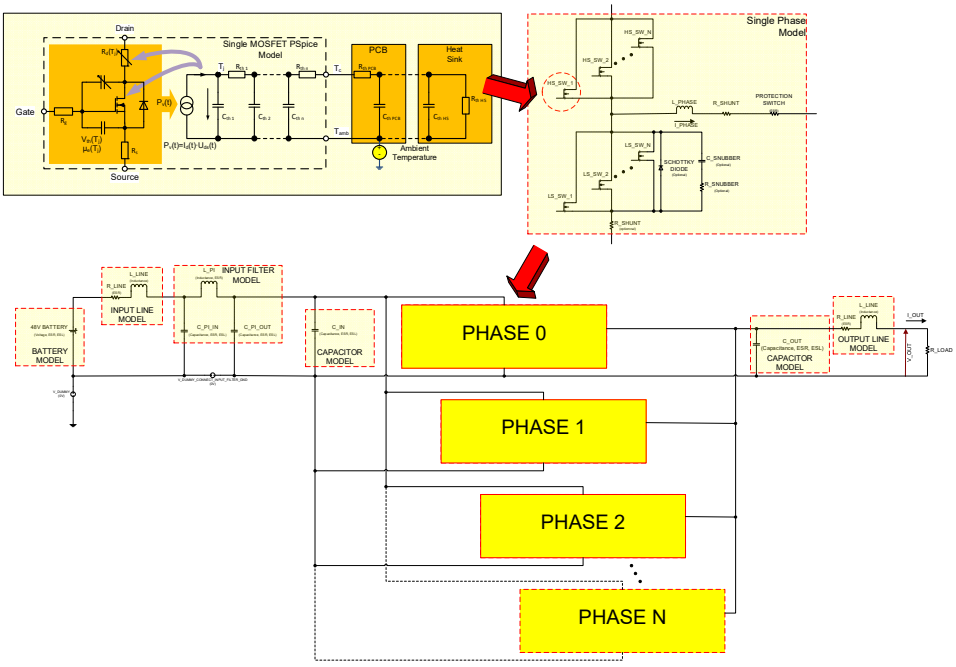

Fig. 1 Setup for concept investigations with SPICE simulations

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*******************************************************************************
*                                                                             *
*        Avenue Sweep Parameter Overview, created 2018/07/18 18:15:58         *
*                                                                             *
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Parameter Sweep Information:

  AMBIENT_TEMPERATURE                                  = 105 70
  PROBE_DEPTH                                          = 5
  NR_HS:NR_LS:MOSFET_100V_HIGH:MOSFET_100V_LOW:S5_HIGH:S5_LOW:PR_SW_ESR = 2:2:0:0:0:0:1.9m
  ...                                                  = ... 1:1:1:1:1:1:2.4m 2:2:1:1:1:1:2.4m 1:1:0:0:1:1:2.4m
  ...                                                  = ... 2:2:0:0:1:1:2.4m 2:2:1:0:1:1:2.4m
  SIMULATION WITH RTH                                  = 1
  SCHOTTKY DIODE                                       = 0
  SNUBBER                                              = 0
  TRI_FRQ                                              = 80K 100K
  R_GATE_ON                                            = 5 10 20
  CONST_LOAD                                           = 1
  DUTY_CYCLE                                           = 285m
  SERIAL_SHUNT                                         = 1
  NUMBER_OF_PHASES                                     = 6 8 9 10
  INPUT_FILTER                                         = 1
  OUTPUT_LINE                                          = 1
  INPUT_LINE                                           = 1
  TEST_SIMULATION                                      = 0
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Fig. 2 Typical set of varied parameters in SPICE simulation

As a result of the simulation setup with parameters variations, a couple of hundreds of simulation runs are executed in parallel on the computing farm, automatically generating efficiency map tables. One example efficiency map table created for typical operation conditions is shown in Fig. 3.

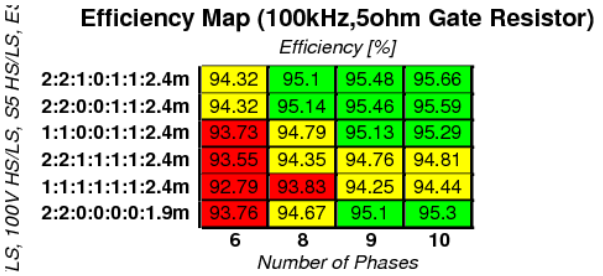

Fig. 3 DC/DC Efficiency Map (@ 3 kW Constant Load, 100 kHz, Rg 5.0 Ω, Ta 105°C)

It should be mentioned that with 5-port MOSFET behavioural SPICE models (next to gate, drain and source as electrical ports, there are junction temperature and case temperature as thermal ports as well) not only electrical, but also thermal behaviour of semiconductors is modelled, enabling proper dimensioning of PCB layers w.r.t. PCB layer thickness, area of layers and their inter-connection (via) and aluminium heatsink for passive air cooling. Typical waveforms of junction port (used just for temperature observing) and case port (connection to the PCB) are shown in Fig. 4.

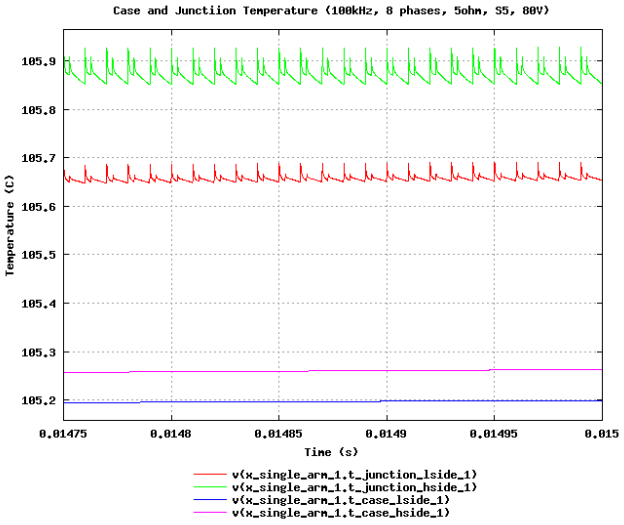

Fig. 4 Case and Junction Temperature (@ 3 kW Constant Load, 100 kHz, Rg 5.0 Ω, Ta 105°C, High Side and Low Side MOSFET in S5/80 V Technology, 8 Phases in Parallel)

2.2 DC/DC Converter Topology

Based on requirements defined in section 1 (redundancy, modularity, safety) and feasibility study made based on SPICE simulations described in section **Fehler! Verweisquelle konnte nicht gefunden werden.** (efficiency, switching frequency) decision is made to implement topology shown on Fig. 5.

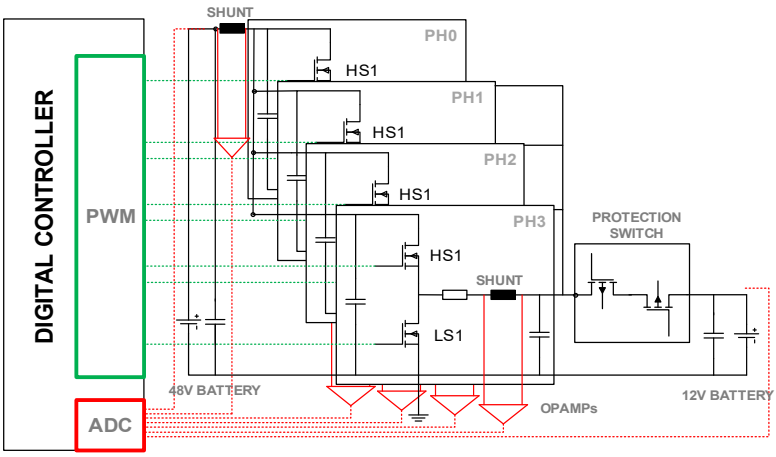

Fig. 5 Block diagram of an automotive 48 V/12 V DC/DC converter's single channel consisting of 4 phases and common protection switch

Fig. 5 shows the block diagram of a multiphase buck-boost converter with digitally implemented control algorithm. Ever increasing electrification of passenger vehicles just recently recognized the need for digital control of DC/DC converters, but is still strictly limited to the commercially available low cost automotive microcontrollers. Although the cost is the leading argument to stay with proven analog converters, the possibility of using a single device - microcontroller to take over not only the role of computing the control algorithm for the multiphase system at switching frequencies in the range of 100 kHz, but also the role of communication, supervision tasks and important safety measures to support the system safety concept, makes it a solution for safety critical applications.

Digital current mode controller has been analysed in multiple references [PM05], however usually reported with FPGA implementation. One of the objectives of this paper is to present the experimentally proven controller design and implementation in the converter in Fig. 6. The controller has standard two-loop architecture: an outer,

slower voltage loop (target bandwidth (BW) of PI controller of 1 kHz) and inner, faster current control loops (target BW of PI controller of 10 kHz) that is simplified shown in Fig. 7.

A well-known disadvantage when sampling the current only once per switching period (used with average current control mode Fig. 8) is the fact that reaction to a current transient takes at least one switching period [PM05]. Furthermore, average current control mode unfortunately does not allow direct cycle-by-cycle current limitation.

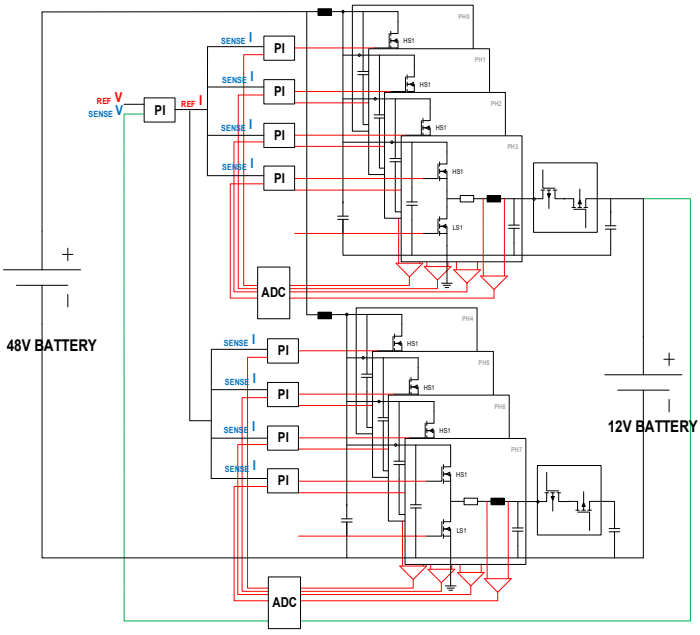

Fig. 6 Block diagram of an automotive 48 V/12 V DC/DC 3 kW converter built of 2 channels (each single channel consisting of 4 phases and common protection switch) including common voltage and multiple phase current loops

Since the short current protection between two automotive board nets is an essential requirement in the system presented in this paper, two-level overcurrent protection is implemented. The protection is implemented for each channel (consisting of 4 phases) separately using shunts and amplifiers presented in a channel in Fig. 6. The first level is the phase current limitation based on phase current sense signals brought to the ADC. When any of phase current sense signals reaches the pre-defined overcurrent threshold, the protection is tripped and the complete channel containing the phase affected by the overcurrent event is disconnected through the corresponding disconnects switch (Fig. 6). In addition, the PMW signals are stopped from being propagated to the gate drivers. The

first level of the current protection can only detect the overcurrent event that can also be observed through the inductor including short circuit protection between 48 V and 12 V side. Therefore, the second level of current protection had to be implemented for detection of overcurrent events that possibly do not affect the phase inductors. A single current sensing resistor as proposed in [CLH16, HS16] is used for this purpose in the common 48 V line of each of two separate channels presented in Fig. 6. When the set limit is reached, the emergency stop of the microcontroller is activated. The activation of this emergency stop, immediately switches the PWM output, and channel enable signal, to 3-state without the intervention of the CPU. This enables the external pull down resistors to set the DC/DC in a safe state and avoid hardware damages.

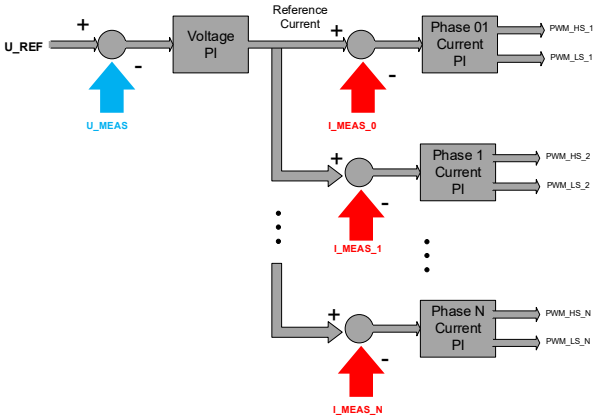

Fig. 7 Simplified block diagram of control method with common voltage and multiple phase current control loops

Due to the fact that the duty cycle in both buck and boost operating mode for the voltage ranges of the presented system is not expect to increase over 0.5 in the worst case, it is assured that the ripple peaks of phase input currents of a channel consisting of a four phases will be faithfully represented in the sensed total input channel current signal (Fig. 9).

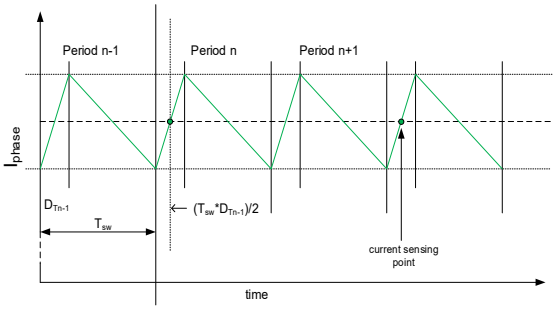

Fig. 8 Illustration of average current sensing

Therefore, in the case of channel input current sensing the sensed signal is not forwarded to ADC but compared in an analog way to the threshold. The comparator output is further brought to the input of the microcontroller to be handled with higher priority.

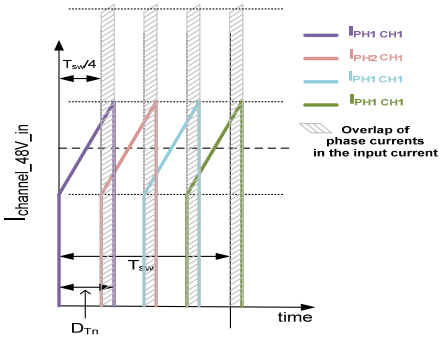

Fig. 9 Fragments of input channel current

2.3 Phase Shedding

Phase shedding is an often used approach to improve the efficiency of the multiphase converters at light load by adapting the number of phases to the load level based on either pre-measured or real-time information of the system [ATA16, GZC09, SL13, GB16, PM05]. During the phase shedding when the number of phases is being reduced by one, in the system presented in this paper it is important to avoid excessive current overshoots that could trip the protection and unnecessary turn-off the phases. In an analog implementation and when using peak current control, this overshoot will not appear. Current overshoot can be damped by adjusting the parameters of the current PI regulator. However this makes the regulator to react slower and can affect the regulation

speed in nominal operating conditions. Also, with this method only limited damping of the current overshoot is possible still maintaining the danger of tripping current protection during phase number reduction. To avoid the deterioration of converter's dynamic while avoiding any unintentional protection tripping, the simple method is proposed in this paper. After receiving the command for phase number reduction, the controller does not immediately stop the PMW signals propagation to the gate drivers of the phase to be turned off. It first reduces the current reference of this particular phase per ramp to 0 A. This is the moment in which the phase disable signal can be safely sent. This action does not reduce the duty cycle of the particular phase to 0 since it would in certain cases lead to the negative current through the phase.

3 Control Algorithm Development

To overcome control algorithm challenges (phase interleaving, current balancing in 8 phases, load dynamics, modularity/phase shedding, available µC computational power) different multi-phase DC/DC Matlab/Simulink models were developed. State-Space Averaging model whose structure is shown in Fig. 10 is used to determine PI parameters of controller around nominal operating point.

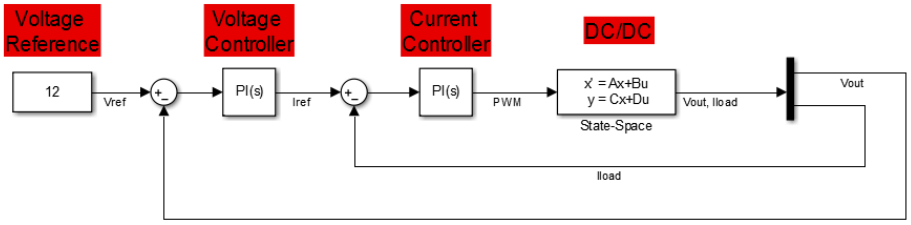

Fig. 10 Block diagram of a DC/DC converter using State-Space Averaging method

On the other side, for fine tuning, to determine the of influence of variations of HW manufacturing parameters (inductance, shunt resistance, PCB) and most important for investigating the response of the system on the disturbances (e.g. load change) Matlab/Simulink SimPowerSystems toolbox models (shown on Fig. 11) are used.

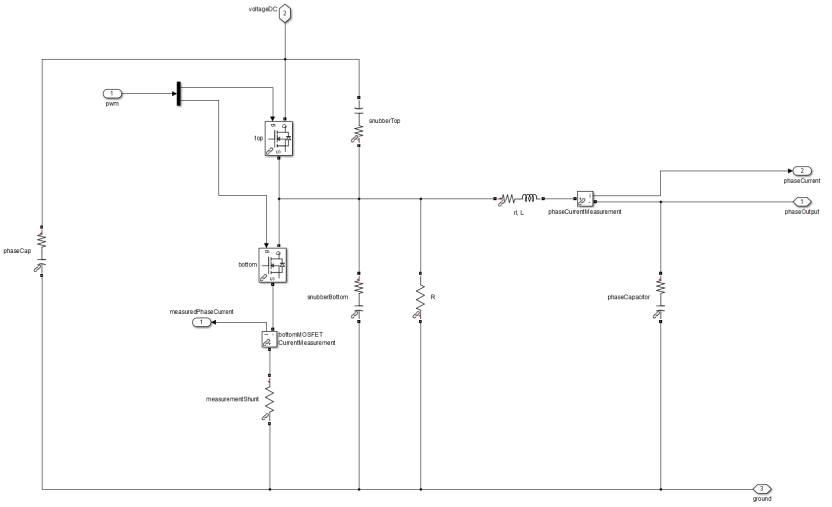

Fig. 11 Block diagram of one phase of a DC/DC converter using Matlab/Simulink SymPowerSystems toolbox

As a result of the control algorithm development, control structure depicted in Fig. 7 is implemented. In the "outer" control loop, the voltage controller (based on difference between reference and measured voltage) generates reference current and in "inner" loop, one current controller per phase (based on difference between reference and measured phase current) generates PWM duty cycle (separately for each phase). Main reason for having separate PI current controllers for every current control loop is in the fact that due to HW manufacturing variations, when using the same duty cycle for every phase, the difference in currents per phase at nominal load could be even 25-30% (proven in simulation and experimentally) what would lead to overheating, deteriorate of performance and finally physical destroying of power converter. On the other hand, increased number of PI controllers had as a consequence that the CPU computational power of a selected µC (again, typically automotive, the selection of µC was cost-driven) was not enough to calculate the duty cycle in real time at 100 kHz, forcing as a final consequence that the duty cycle is calculated and updated just at every second switching cycle (50 kHz -> 20 µs). Finally, by means of MathWorks' Embedded Coder C code is automatically generated and flashed to the TC264D.

4 Implementation in Microcontroller

4.1 Phase shift

As mentioned before in section 2.2, the control of the 8 phases is split in 2 channel groups, each channel having 4 phases. In order to minimize the ripple, the phases are

equally shifted as shown in the Fig. 12. The two channels are shifted by one 8th of a period, whereas within a channel all phases are shifted by a 4th of a period.

The PWM is configured to center aligned mode, so that the distance between all phases center is constant whatever the duty cycle settings. This is required to enable a synchronous phase current measurement by the SAR ADC.

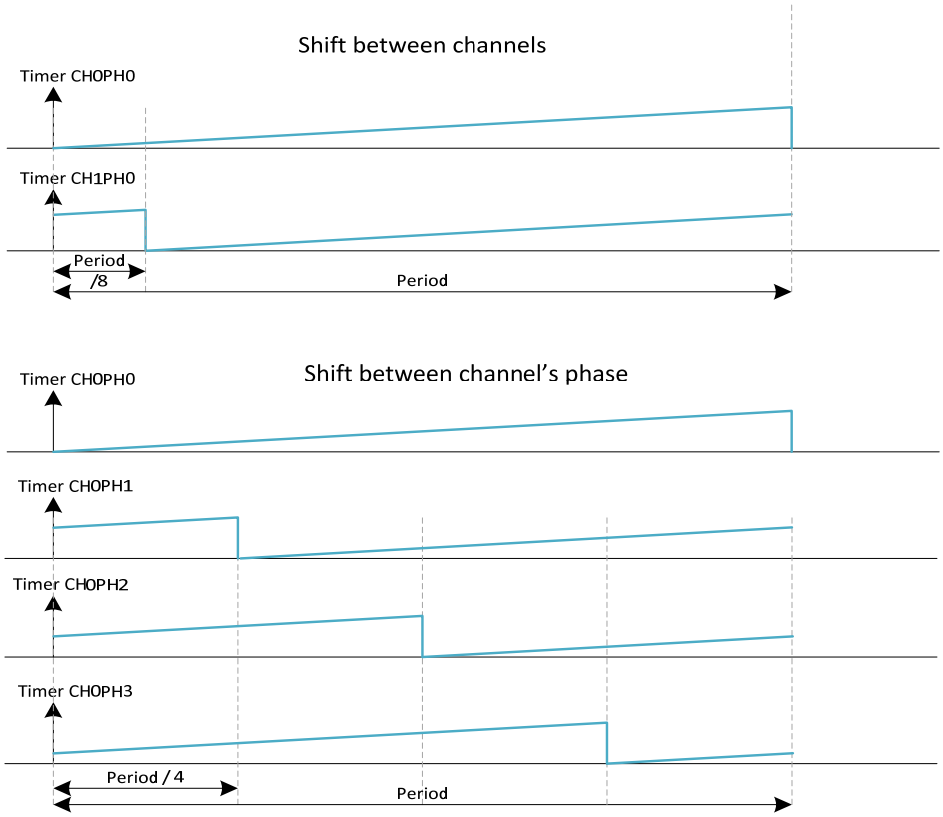

Fig. 12 Phase shift

4.2 Synchronisation and Timing

The phase currents are measured synchronously to the PWM by a SAR ADC. The sampling point is set so that the phase average current value is measured, and has been chosen to be around the middle of the low side switch, ON state. To achieve that, as shown in Fig. 13, an additional timer running at 4 times the PWM frequency triggers periodically the ADC so that the different phase currents are converted one after each other. When each phase current conversion is finished, an interrupt on CPU 0 is

triggered to scale the acquired phase current and update the PWM with new value calculated within the last 20 us. Additionally the interrupt triggered by the phase 0 current conversion every 20 us, triggers an interrupt on CPU 1 which starts the duty cycle calculation algorithm (code automatically generated by means of MathWorks' Embedded Coder) to calculate the new duty cycles to be applied.

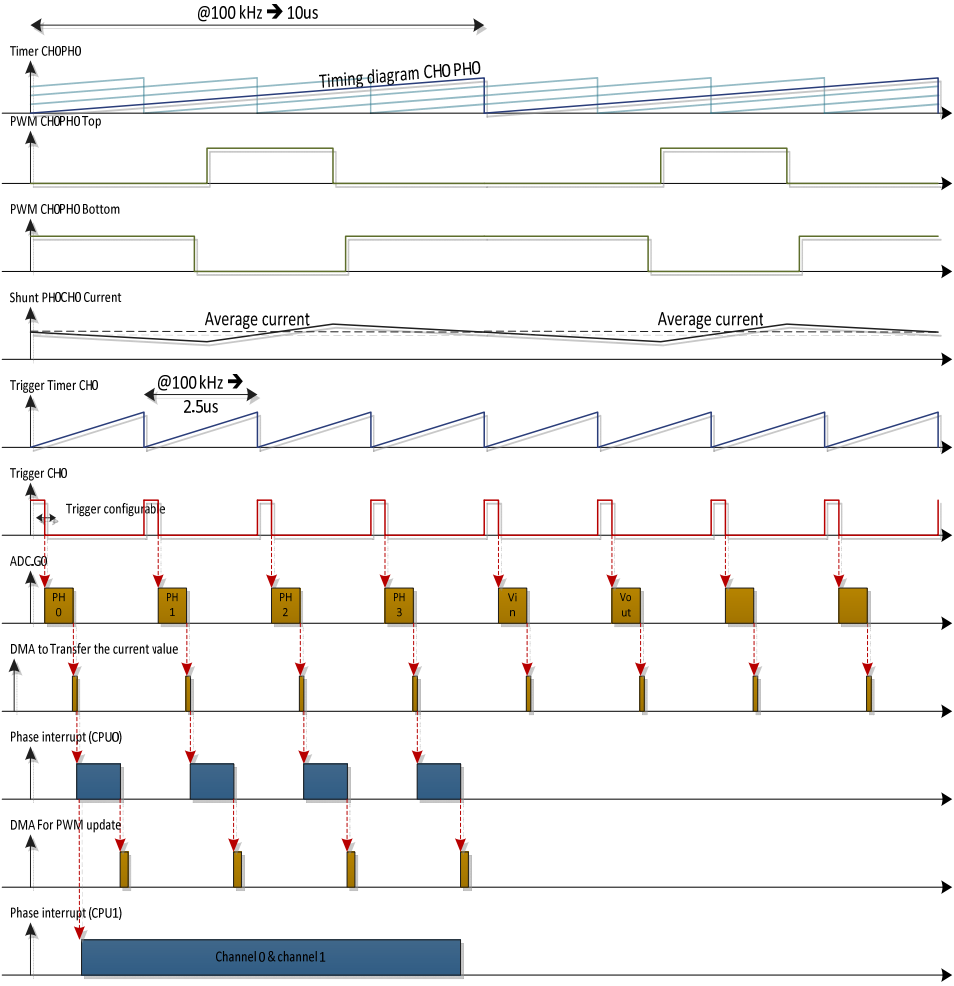

Fig. 13 Time diagram for channel 0

The Fig. 14 shows the timing when the both channels are enabled, in this configuration about 50% of the AURIX TC264D computational power is used.

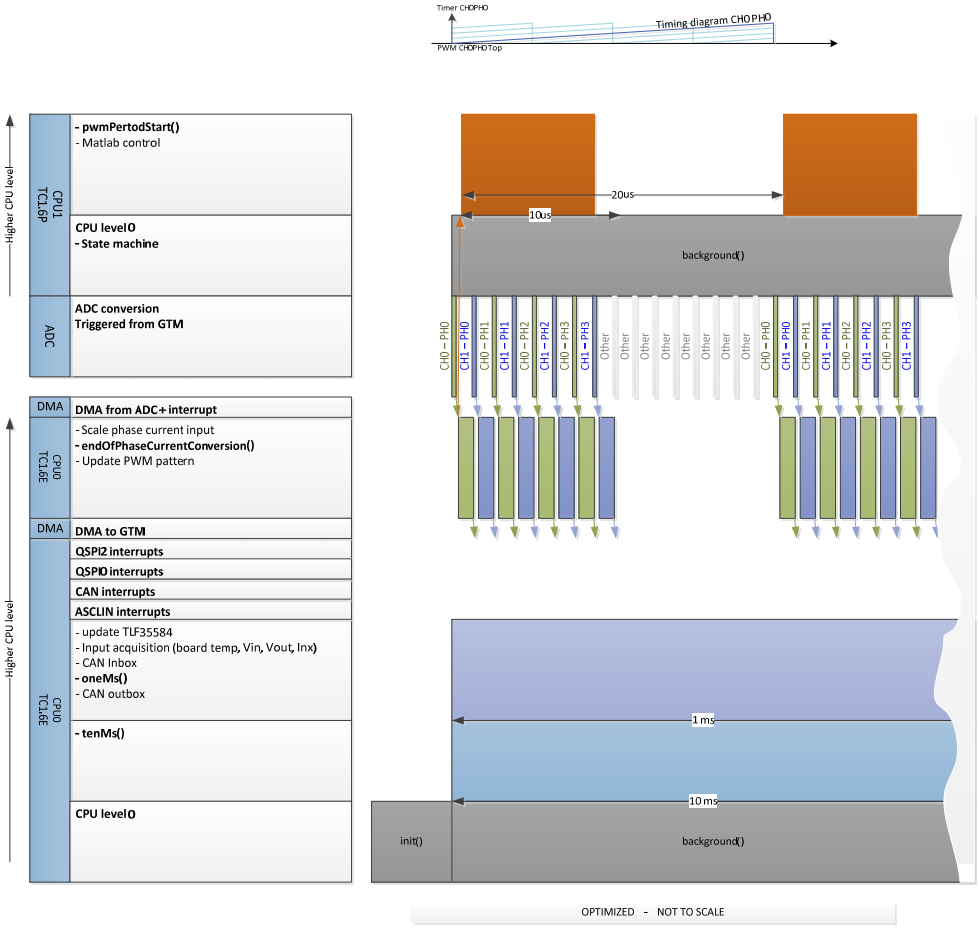

Fig. 14 Time diagram for 2 channels / 8 phases

5 Experimental Results

Efficiency pre-measurements as shown in are used for implementation of phase shedding (Fig. 15). The thresholds for changing the number of phases are determined and fixed in the control algorithm. By setting the threshold based on the pre-measured efficiency, very smooth efficiency curve (Fig. 16) can be achieved in the direction of load increase. The hysteresis is implemented needs to be implemented to avoid consecutive phase turn on/ off until the load reaches steady state.

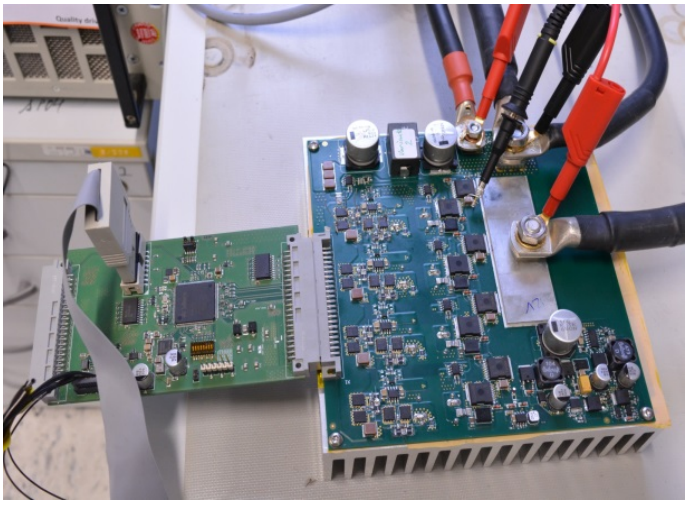

Fig. 15 Lab setup – 1.5 kW 4 phases passive air cooled power stage controlled by µC stage; Lab voltage source and electronic load are used in place of 12 and 48V batteries

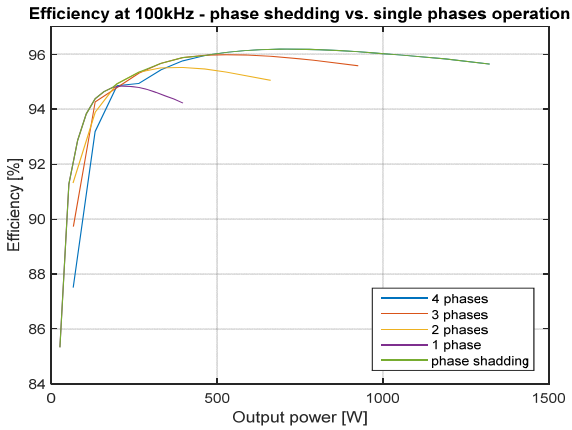

Fig. 16 Light load efficiency improvement due to phase shedding

6 Summary

The idea of extending the automotive on-board power network by 48 V voltage level brings the need for a power converter that will tie the 12 V and 48 V board nets together to enable safe and efficient energy exchange between them. The coupling is

performed through the DC/DC converter with power rating of up to 3 kW. As such power rating of the converter imposes the need for the high currents at 12 V side, Infineon Technologies presented a novel multiphase interleaved concept for 48 V/12 V DC/DC converter having BOM of up to 90% of in-house semiconductors content including power switches for switching and protection (OptiMOS™ in 100 V and 40 V technology), MOSFET drivers, microcontroller (AURIX™ TC264D) and power supply/communication ICs) – challenges like reaching high conversion efficiency at 100 kHz switching frequency and development of complex control algorithm are solved by using electrical/thermal co-simulation and automated code generation. Infineon's automotive best-in-class $R_{ds,on}$ OptiMOS™ switches offers a solution that not only improves thermal distribution and reduces the size of passives, but also has a tremendous effect on modularity and scalability of the whole system. The possibility to isolate only a part of the converter in case of a single failure is the key benefit for the safety critical system such as the 48 V to 12 V converters. By using AURIX microcontroller that integrates all the control and safety functions in one chip, the concept presented here offers an integrated and compact solution that at the same time successfully fulfills strict requirements regarding safety and efficiency.

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