Douglas Cunningham, Petra Hofstedt, Klaus Meer, Ingo Schmitt (Hrsg.): INFORMATIK 2015
Lecture Notes in Informatics (LNI), Gesellschaft für Informatik, Bonn 2015

Reducing Power Consumption in Fault Tolerant ASICs

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Abstract: Fault tolerance techniques have been traditionally used for specific applications such as space, avionic, or nuclear where the reliability is of utmost importance. Moreover, nowadays the reliability of nanoscale CMOS processes is reduced, and the power optimization goes beyond the standard worst-case boundaries. As a consequence, fault tolerance became the important factor also for the main stream industry. Handling faults is connected with some sort of redundancy either in hardware, timing, information, or by combination of previously defined methods. The immediate consequence of the redundancy is increased power consumption. As an example, the traditional N-modular redundancy techniques, such as TMR (triple modular redundancy) end up in the power overhead of about 300-400% of original non-protected system. In order to limit the overhead the additional methods and techniques need to be applied. In this presentation the relevant state-of-the-art methods for reducing power consumption in fault tolerant chips will be presented. This will include the global overview of the traditional methods (such as improvements of TMR/DMR schemes) and novel methods for low-power ASICs (such as RAZOR). Moreover, the methods at different abstraction layers proposed at IHP for handling the power optimization in fault-tolerant ASICs will be presented. At the RTL level, selective fault tolerance can be applied limiting overhead by 50% with still protecting 20% of the inputs. Additionally, for the memories the overhead can be reduced by utilizing specific error correction codes. Finally, the fault tolerance can be introduced on application demand, dramatically reducing the power consumption when it is not needed. This can be performed on the pipeline level or even at the level of multi-processors. Such an example will be shown and IHP's FMP adaptive multi-core platform will be presented.

Keywords: fault tolerance, TMR, low power

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